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LSI Logic Corporation
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Milpitas, CA 95035

Date December 2, 2004

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To: US PTO

Mail Stop Status Request

TC 2825

Fax No. 703-872-9306

Phone No.

CC:

From: Connie del Castillo

Intellectual Property Paralegal

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REMARKS:

☐ Urgent

☐ For your review

☒ Reply ASAP

☐ Please comment

Application Number: 10/697,357
Filing date: October 29, 2003
First named inventor: Viswanathan Lakshmanan et al.
Attorney docket number: 03-1772 / 81610

Transmitted herewith for filing via facsimile:

- Status Request Letter

Pursuant to 37 C.F.R. 1.8, I hereby certify that this correspondence is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date indicated below:

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Connie del Castillo

Signature

Connie del Castillo

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Viswanathan Lakshmanan et. al.

Serial No. :

10/697,357

Filed :

October 29, 2003

For :

Method Of Partitioning An Integrated Circuit Design For Physical Design Verification

www.pearsoned.com

Group Art Unit: 2825

Examiner :

Atty Docket : 81610 / 03-1772

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STATUS REQUEST

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir,

Applicants request a status of the above referenced application. Please mail the status notification to the address stated below.

Respectfully submitted,

Peter Cott

Peter Scott, Ph: [+1] 408-433-7191

Reg. No. 33,279

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